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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	Jooyoung Yoon, <i>et al.</i>
Serial No. 10/798,998	Filing Date: March 12, 2004
Title of Application:	Method for Forming Pattern in Semiconductor Device
Confirmation No. 6864	Art Unit: 1756
Examiner	

Commissioner for Patents
Post Office Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement by Applicants

As a means of complying with the duty of disclosure set forth in 37 CFR §1.56, Applicants list the following references (copies of the listed patents and papers enclosed).

U.S. Patent Documents				
Exam. Initials	Class/ Subclass.	Document No.	Date	Name
	437/40	5,512,500	4/1996	Oyamatsu

Mailing Certificate: I hereby certify that this correspondence is today being deposited with the U.S. Postal Service as *First Class Mail* in an envelope addressed to: Commissioner of Patents and Trademarks; Post Office Box 1450; Alexandria, VA 22313-1450.

February 16, 2005

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Foreign Patent Documents			
Exam. Initials	Document No.	Date	Country
	0098994 B1	7/1995	Republic of Korea [with English abstract]
	1997-51846A	7/1997	Republic of Korea [with English abstract]
	0147771 B1	2/1998	Republic of Korea [with English abstract]

The listed patents pertain in a general way to the subject matter of the application, but are not necessarily considered to be analogous prior art.

Applicants submit that each item contained in this IDS was first cited in a communication (copy enclosed) from a foreign patent office in a counterpart foreign application.

Respectfully submitted,

February 16, 2005

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